## REMARKS

Reconsideration and allowance are requested.

The Examiner is requested to have all records in the USPTO databases reflect the fact that the last name of the first named inventor is "Blasco Allue" and not simply "Allue". Confirmation is requested.

Claims 1, 2, 15, 16, and 29 stand rejected under 35 U.S.C. 102 as being anticipated by Dervisoglu et al (6,964,001). This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Dervisoglu fails to satisfy this rigorous standard.

Dervisoglu describes an integrated circuit with a processor for test and debug of user-definable logic plus external interface between the test/debug circuits and the component pins. The external interface may be via an existing test interface, or a separate serial or parallel port. Test and debug circuits contain scan strings used to observe states in user-definable logic or provide pseudo-random bit sequences to user-definable logic. The test and debug circuits also contain an on-chip logic analyzer for capturing sequences of logic states in user-definable circuits.

Regarding claims 1 and 15, Dervisoglu fails to disclose an integrated circuit with a processor for performing both *non-diagnostic* data processing operations under program instruction control and *diagnostic* data processing operations under program control "including

accessing said diagnostic data relating to said data processing circuit independently of said data processing circuit." The control unit in Dervisoglu is dedicated to its diagnostic function—it does not also perform non-diagnostic data processing operations.

Using one processor to perform both non-diagnostic and diagnostic operations on the IC is more efficient and uses less chip space. Moreover, while the data processing circuit under investigation may, for example, be halted to provide halting mode debug, have taken an exception to provide monitor mode debug, or have been subject to code profiling diagnostic data capture while still executing program instructions, the processor being used to perform the diagnostic operations remains active and queries the captured diagnostic data on-chip using high speed and efficient communication mechanisms.

Lacking the combination of features recited in the independent claims, the anticipation rejection is improper and should be withdrawn. Chen does not remedy the basic deficiency in Dervisoglu. The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

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